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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,178	02/13/2004	Jian-Shen Yu	10929-US-PA	2177

31561 7590 03/28/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, JIMMY H	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,178	YU ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 8-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 8* is/are rejected.

7)☒ Claim(s) *9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 02/15/2007.

Claims 3 and 8-12 are currently pending in the application. An action follows below:

Drawings

2. The drawing was received on 02/15/2007. This drawing is acceptable.

Claim Objections

3. Claim 3 is objected to under 37 CFR 1.75(a) because although this claim meets the requirement 112/2d, i.e., the metes and bounds are determinable, however, the following changes should be made: "**one of**" in line 12 should be delete because a target signal must have two levels. Appropriate correction is required.

As to claim 2, as noting in Fig. 9, Yamazaki discloses the first level shifter circuit receiving the clock signal (CLK) during a period, which inherently begins when a user turns a display on and ends when a user turns the display off (i.e., a predetermined period).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 is under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art, hereinafter AAPA, and further in view of Yamazaki et al. (US 6,392,628 B1), hereinafter Yamazaki.

As to claim 3, as noting in Fig. 1 and paragraph 0008 of the specification, AAPA discloses a driving stage for an LCD driving circuit (see paragraph 0008), the driving stage being part of the LCD driving circuit in a cascade fashion, the driving stage comprising: **a clock input terminal (CLK in** terminal; see Fig. 1), for receiving a clock signal (CLK) having **a first original level (3V)** and **a second original level (GND or 0V)**; **a level shifter** (a circuit including elements 105 and 110; see Fig. 1) coupling to the clock input terminal (CLK in) for receiving the clock signal (CLK) from the clock input terminal, operating at **a first target level** (a positive voltage **VDD**) and **a second target level** (a negative voltage **VSS**), for amplifying the clock signal to **a relay signal** (an output of the element 110, see Fig. 1) having **a first relay level (VDD)** and **a second relay level (VSS)**; and **an output buffer (115)** coupling to the level shifter (110) for receiving the relay signal from the level shifter and operating at the first target level (VDD) and the second target level (VSS) for amplifying the relay signal to a target signal having the first target level (VDD) and the second target level (VSS); wherein the first original level (3V) is higher than the second original level (GND); the first target level (VDD) is higher than the second target level (VSS); the first relay level (VDD) is higher than the first original level (3V) and is the same as the first target level; and the second relay level (VSS) is lower than the second original level (GND) and is the same as the second target level. Accordingly, AAPA discloses all the claimed limitations except that the first relay level is lower than the first target level and the second relay level is higher than the second target level, as presently claimed.

However, Yamazaki discloses **a level shifter** (a circuit including a first level shifter circuit and a shift register circuit; see Fig. 9) for amplifying the clock signal (CLK) to a relay signal (an output signal of the shifter register circuit, see Fig. 9) that swings between **a first**

relay level (+5V) (see Fig. 9; col. 22, lines 35-38; col. 1, line 63 through col. 2, line 3; and col. 3, lines 19-37) and **a second relay level (-5V)** (see Fig. 9; col. 22, lines 35-38; col. 1, line 63 through col. 2, line 3; and col. 3, lines 19-37) and , by using the first level shifter circuit and the shift register circuit, wherein the first relay level (+5V) is higher than the second relay level (-5V); and an output buffer (a second level shifter circuit) amplifying the relay signal to the target signal (an output signal of the second level shifter circuit, having a first target level (10V) and a second target level (-10V)); wherein **the first relay level (+5V) is** higher than the first original level (3V) and **lower than the first target level (+10V)** and **the second relay level (-5V) is** lower than between the second original level (GND/0V) and **higher than the second target level (-10V)**. Accordingly, the claimed limitations are read in the Yamazaki reference. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the level shifter of AAPA to generate the relay signal having the first relay level being lower than the first target level and the second relay level being higher than the second target level, in view of the teaching in the Yamazaki reference, because this would at least reduce the power consumption, as taught by Yamazaki (see col. 10, lines 3-8).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Yamazaki as applied to claim 3 above, and further in view of Maekawa et al. (US: 5,646,642), hereinafter Maekawa.

As to claim 8, as discussed in the rejection to claim 3 above, AAPA in view of Yamazaki discloses all the claimed limitations except for a dynamic register, as defined in claim 8. However, Schmidt discloses a related driving stage comprising a dynamic register (a detecting/offsetting circuit 1A, see Fig. 1) receiving a clock signal (CK1) and determining

whether to provide the clock signal to the level shifter (a level shifting circuit 2, see Fig. 1, col. 4, line 56) according to a control signal (a signal is supplied to the gate electrode of TFT mpA, see Fig. 1), see col. 4, lines 50 through col. 5, line 27). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the dynamic register in the driving stage of AAPA, in view of the teaching in the Maekawa reference, because this would provide a level converting circuit which operate stably for any clock signal having a low amplitude, as taught by Maekawa.

Allowable Subject Matter

7. Claims 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if overcome the claim objections above. See the statement of reasons for the indication of allowable subject matter in the Office Action dated 11/20/2006.

Response to Arguments

8. It is noted Applicant that the drawing objection, claim objection, and the rejections under 35 USC 112, first and second paragraphs, in the previous Office action dated 11/20/2006, have been rendered moot in light of the amendments to claims 3 and 8-10 and the cancellation to claims 4-7. These objections and rejections in the previous Office action dated 11/20/2006 are hereby withdrawn.

9. Applicant's arguments, see pages 8-9 of the amendment filed on 02/15/2007, with respect to the rejections under 35 USC 102 and 103 in the Office Action dated 11/20/2006, have been fully considered and are persuasive in light of the amendment to independent claim 3. However, upon further consideration, the new grounds of rejections are made above.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
March 22, 2007

Jimmy H. Nguyen
Primary Examiner
Technology Division: 2629

Approved by
JHW
3/16/07

Replacement Sheet

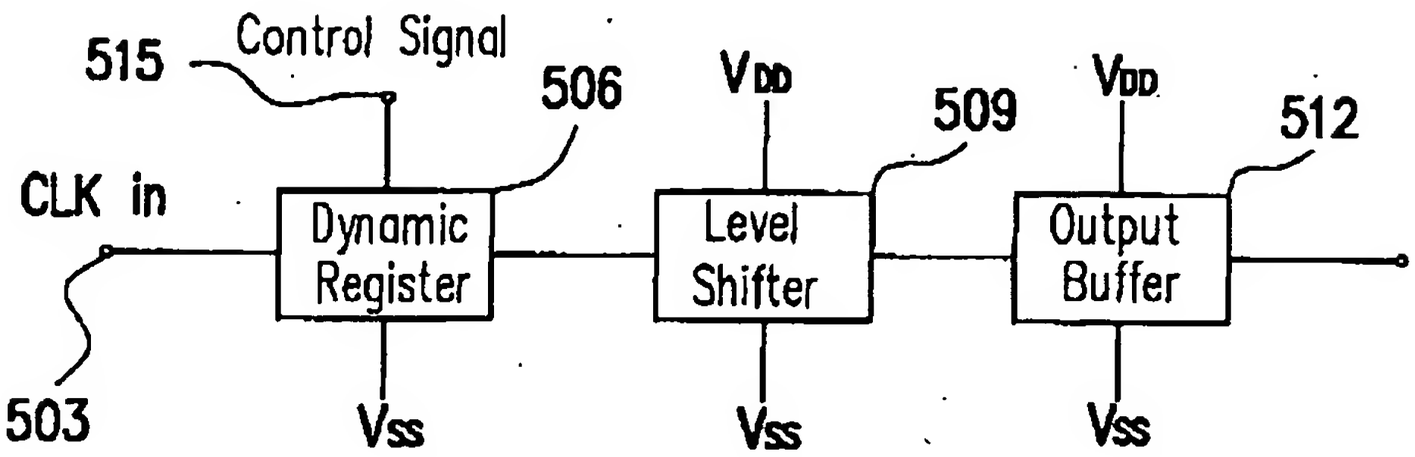

FIG. 5A

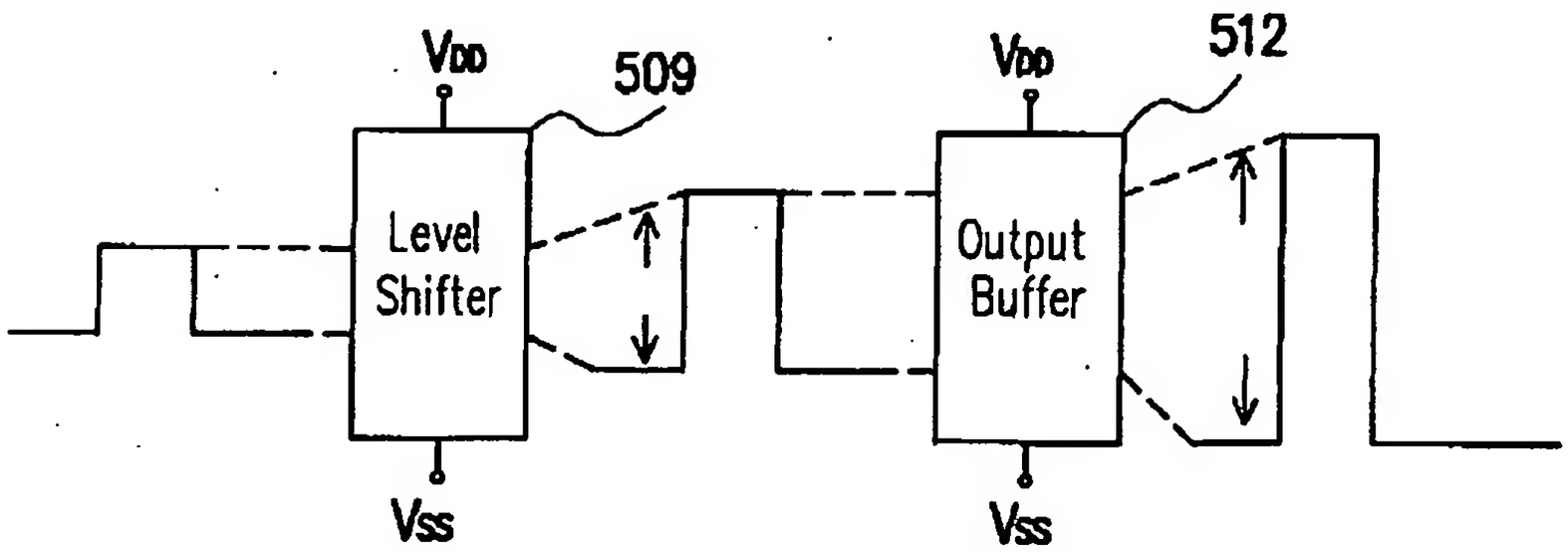

FIG. 5B